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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/972,576	10/05/2001	Petrus Hubertus Cornelis Magnee	NL 000549	4658
24738	7590	06/01/2004	EXAMINER	
PHILIPS ELECTRONICS NORTH AMERICA CORPORATION INTELLECTUAL PROPERTY & STANDARDS 1109 MCKAY DRIVE, M/S-41SJ SAN JOSE, CA 95131			IM, JUNGHWAM	
		ART UNIT	PAPER NUMBER	
		2811		

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	09/972,576	MAGNEE ET AL.	
	Examiner Junghwa M. Im	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 12 March 2004.
- 2a) This action is FINAL.      2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-5, 9 and 10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-5, 9 and 10 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All
  - b) Some \*
  - c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                    | Paper No(s)/Mail Date. _____.   |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____.                                   |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless—

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Pao et al. (US 4344081).

Regarding claim 1, Figure 10 of Pao shows a semiconductor comprising a substrate layer (10) with an upper surface and a lower surface, the substrate layer being a first conductivity type (N); a first buried layer N (a left side portion of the layer 12) in the substrate, extending along said lower surface below a first portion of said upper surface of said substrate layer, and a second buried layer N (a right side portion of the layer 12) in the substrate, extending along said lower surface below a second portion of said upper surface of said substrate layer; a first diffusion region (20; col.4, lines 44-46) in said first portion of said substrate layer, being of a second conductivity type (P) opposed to said first conductivity type (N) and having a greatest depth at a first point along a width of the first diffusion region and having a lesser depth at a second point along said width; and a shallow region (32) in said first portion of said substrate layer, being of said first conductivity type (N) and being o top of said second point of the first diffusion region but not on top of said first point of the first diffusion region.

a second diffusion region (22; col.4, lines 44-46) in said second portion of said substrate layer, being of a second conductivity type (P).

Regarding claim 2, Figure 11 of Pao shows the first diffusion region (20) is a base of a bipolar transistor, said shallow region (32) is an emitter of said bipolar transistor and the first buried layer (12) is a collector of said bipolar transistor.

Regarding claims 3 and 9, the device shown in Figure 10 of Pao inherently shows the second diffusion region (22; P type) is an anode of a pn diode and the second buried layer (a right side portion of the layer 12; N type) is a cathode of the pn diode (col.7, lines 33-36).

Regarding claim 4, Figure 10 of Pao shows the first buried layer is connected to said second buried layer, and the first and second buried layers are manufactured in the same step.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pao in view of Harmel et al. (US 5410177), hereafter Harmel.

Regarding claim 5, Figure 10 of Pao shows the most aspect of the pending claim except "a channel stopper region in said second portion of said substrate layer; the channel stopper region being of said first conductivity type, for electrically isolating said second portion of said substrate layer within the substrate, wherein said channel stopper region is arranged to extend

substantially as an extended channel stopper region in between said second diffusion layer and said second buried layer."

Figure 1a of Harmel shows a channel stopper layer (CS; N type) formed in a buried region (a left side portion of the region 9; a portion having an anode A; N type) and the channel stopper region is arranged to extend substantially in between the diffusion layer for the anode (A) and the buried layer (a right portion of the buried region 9; a portion with the BJT formation).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Harmel into the device of Pao in order to have a channel stopper layer in the specified region as recited in the claim since an addition of the channel stopper to the specified region would alleviate an effort to adjust the breakdown voltage with a manufacturing advantage.

Note that pending claim recites that a channel stopper formation in the in said second portion (a portion with a diode formation) of the substrate layer; the channel stopper region being of said first conductivity type (N; the same type to the substrate and the buried layer), for electrically isolating said second portion of said substrate layer within the substrate, wherein said channel stopper region is arranged to extend substantially as an extended channel stopper region in between said second diffusion layer (a region with an anode formation) and said second buried layer (a right side portion of the layer 12).

Regarding claim 10, Figure 10 of Pao shows the most aspect of the pending claim except a channel stopper region between said second diffusion layer and said second buried layer.

Figure 1a of Harmel shows a channel stopper layer (CS; N type) formed in a buried region (a left side portion of the region 9; a portion having an anode A; N type) and the channel stopper region is arranged to extend substantially in between the diffusion layer for the anode (A) and the buried layer (a right portion of the buried region 9; a portion with the BJT formation).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Harmel into the device of Pao in order to have a channel stopper layer in the specified region as recited in the claim since an addition of the channel stopper to the specified region would alleviate an effort to adjust the breakdown voltage with a manufacturing advantage.

#### *Response to Arguments*

Applicant's arguments filed March 12, 2004 have been fully considered but they are not persuasive.

First, Applicant argues that the instant invention and prior art, Pao reference are not related. Note that both of the instant invention and Pao's device are regarding a power transistor with a diode structure is incorporated. In particular, Applicant argues that "there is a particular feature in that simultaneously with the transistor (2), the protection diode (9) is formed." And Examiner assumes this aspect can be read a corresponding circuit in Fig. 1 of the instant invention. Note that Fig.11 of Pao shows a portion of a circuit configuration identical to the Fig. 1 of the instant invention except the passive elements.

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Second, starting on page 2, Applicant argues that "Applicant builds both a bipolar transistor and a protection diode, **simultaneously**." Note that the instant invention is regarding a device and a patentable weight is carried on a device structure regardless of how the structure is formed.

Applicant continues to argue the instant invention discloses "the first buried layer refers to the buried layer of the transistor... the second buried layer refers to the buried layer of the diode." Then, Applicant further argues that two buried layers of Pao are distinct regions, one for a transistor and one for a diode. Examiner fails to understand this argument.

In addition, Applicant argues Examiner misinterpreted the claimed features in referring to buried layer such as the first buried layer as "a left side portion of the layer 12" and the second buried layer as "a right side portion of the layer 12." However, the pending claim 1 also recites "a *first buried layer* (12) ... below a *first portion* ... of said substrate layer (13) ... a *second buried layer* (12) ... a *second portion* .... of said substrate layer (13)"

Finally, Applicant argues that "Were Harmel modified to incorporate the features of Applicant's invention, the original intent of Harmel's invention would be destroyed." Examiner would like to point out that Applicant presents this contention without probative evidence based on the facts.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

  
DR. NADAV  
patent examiner